

## **Analog Bits' Half Power SERDES Demonstrated at DesignCon 16nm IP Supporting PCIe Gen4, HMC and SAS**

**Santa Clara, CA, January 20, 2016** – Come and see Analog Bits' ([www.analogbits.com](http://www.analogbits.com)) new **half power SERDES IP** in the Keysight Technologies booth [#725] at DesignCon 2016. The use of SERDES has been growing dramatically both in terms of number of chips and number of lanes-per-chip. This growth is calling to attention the impact SERDES IP can have on power, size and even chip layout. Analog Bits has revolutionized SERDES IP by cutting the power in half while also supporting multiple standards such as PCIe Gen 4, HMC and SAS while allowing the most flexibility on die placement. Together with electrical compliance testing solutions from Keysight Technologies, customers can implement new chip designs with lower power and higher confidence.

**WHAT: Analog Bits' 16nm half power SERDES IP products**

- Passing JTOL tests using Keysight's latest J-BERT at 16Gbps with less than 750fs RMS jitter
- Multiprotocol including PCIe Gen 3/4, HMC 2.0, 10G-KR.
- Small die size impact
- Location on any die side

**WHEN: DesignCon 2016**  
Expo: January 20-21, 2016

**WHERE: Keysight Technologies booth #725**  
Santa Clara Convention Center  
5001 Great America Parkway  
Santa Clara, CA 95054

**About Analog Bits:** Founded in 1995, Analog Bits, Inc. ([www.analogbits.com](http://www.analogbits.com)), is the leading supplier of mixed-signal IP with a reputation for easy and reliable integration into advanced SOCs. Products include precision clocking macros such as PLLs & DLLs, programmable interconnect solutions such as multi-protocol SERDES and programmable I/O's as well as specialized memories such as high-speed SRAMs and TCAMs. With billions of IP cores fabricated in customer silicon, from 0.35-micron to 16/14-nm processes, Analog Bits has an outstanding heritage of "first-time-working" with foundries and IDMs.

**For more information, please contact:**

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